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PATENT

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Date

August 10, 2001

Denise Sheridan

Denise Sheridan

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants : Daniel B. Penney and Steven So  
Serial No. : 09/836,593  
Filed : April 16, 2001  
Title : BURST COUNTER CONTROLLER AND METHOD IN A MEMORY DEVICE  
OPERABLE IN A 2-BIT PREFETCH MODE

Attorney Docket No.: 500794.01  
Group Art Unit : 2185  
Examiner : Not yet assigned

Box Non-Fee Amendment  
Commissioner of Patents  
Washington, DC 20231

**RECEIVED**  
**AUG 17 2001**

**SUPPLEMENTAL PRELIMINARY AMENDMENT**

**Technology Center 2100**

Sir:

In response to the Notice To File Corrected Application Papers dated June 21, 2001, please amend the application as follows:

**In the Specification:**

Please replace the paragraph beginning at page 2, line 8, with the following rewritten paragraph:

B,   
Burst mode memory devices initially operated by serially accessing the memory cells in an active row. However, with the advent of synchronous DRAM ("SDRAMs") having two separately addressable arrays of memory cells, interleave memory accesses were introduced. In interleave memory accesses, the memory addresses increment by toggling the least significant bit ("LSB") every address, toggling the next to least significant bit ("NLSB") every other